

CLAIMS

What is claimed is:

1 1. A common mode feedback circuit apparatus comprising:
2 a first and a second node defining a differential node pair; and
3 a collective plurality of transconductors including a first plurality of
4 transconductors associated with the first node and a second plurality of
5 transconductors associated with the second node, wherein at least one
6 transconductor of the collective plurality has an adjustable transconductance,
7 wherein the total transconductance of each of the first and second pluralities
8 is nominally halved between any adjustable transconductors and the
9 remaining transconductors of that plurality.

1 2. The apparatus of claim 1 wherein the total transconductance of each of
2 the first and second pluralities is nominally halved between the set of
3 transconductors capable of being decoupled from its associated node and
4 recoupled to a complementary node and the remaining transconductors of
5 that plurality.

1 3. The apparatus of claim 1 wherein each of the first and second plurality
2 of transconductors includes at least one transconductor with an adjustable
3 transconductance.

*repeated
note claim 1
lines 3-5*

1 7. The apparatus of claim 1 wherein each of the first plurality and second
2 plurality comprises 2 transconductors.

1 8. The apparatus of claim 7 wherein every transconductor of the
2 collective plurality has substantially a same nominal transconductance value.

1 9. The apparatus of claim 1 wherein the circuitry is implemented on an
2 integrated circuit semiconductor die.

1 10. The apparatus of claim 9 wherein the integrated circuit is a
2 complementary metal oxide semiconductor (CMOS) integrated circuit.

1 11. The apparatus of claim 1 further comprising:
2 a calibration engine, wherein the calibration engine varies the
3 adjustable transconductance of the at least one transconductor until a sensed
4 differential voltage across the differential node pair is substantially zero.

1 12. The apparatus of claim 11 wherein the calibration engine further
2 comprises a band pass filter to sense the differential voltage at a pre-
3 determined frequency.

3 includes the step of adjusting each of the associated adjustable
4 transconductors until the differential voltage across the differential node pair
5 is substantially zero.

1 18. The method of claim 14 wherein the adjustable transconductors are
2 adjusted by increasing a transconductance of a transistor associated with
3 the first node by an amount δ and decreasing a transconductance of a
4 transistor associated with the second node by the amount δ .

need to be defined

1 19. The method of claim 13 further comprising the step of:
2 c) providing a calibration signal source independent of a common
3 mode node, wherein during calibration the calibration signal source provides
4 a control voltage for the adjustable transconductors, wherein the common
5 mode node provides the control voltage for the remaining transconductors of
6 the collective plurality of transconductors.

1 20. The method of claim 19 wherein the calibration signal source and the
2 common mode feedback block reside on a same integrated circuit die.